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S.S.H.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of
Johannes Roelof Gerardus de Vries
Serial No.:

New York, New York
Date: April 14, 1995
Group Art Unit:

Filed: Concurrently herewith

Examiner:

For: DATA PROCESSING CIRCUIT, MULTIPLIER UNIT WITH PIPELINE, ALU
AND SHIFT REGISTER UNIT FOR USE IN A DATA PROCESSING CIRCUIT

Hon. Commissioner of Patents
and Trademarks
Washington, D.C. 20231

RECEIVED

SECOND PRELIMINARY AMENDMENT

AUG 6 1995

Sir:

Prior to examination, please amend the above-identified
patent application as follows:

IN THE CLAIMS:

Please amend claims 3, 7 and 8 as follows.

Claim 3, line 1, delete "or 2".

Claim 7, line 1, delete "2 or 3,".

Claim 8, line 1, delete "2, 3 or 7,".

Please add new claims 9 - 14.

--9. A circuit according to claim 2, wherein the
integer data comprises 32 bit or 16 bit words.

b
A/ b
10. ^{The} A circuit according to claim 2, in integrated
form.

11. ^{The} A circuit according to claim 3, in integrated
form.